REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25								

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
93-06-07

REVISION LEVEL

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MICROCIRCUIT, DIGITAL, ADVANCED CMOS, OCTAL TRANSPARENT LATCH, WITH THREE-STATE OUTPUTS, TTL COMPATIBLE, MONOLITHIC SILICON

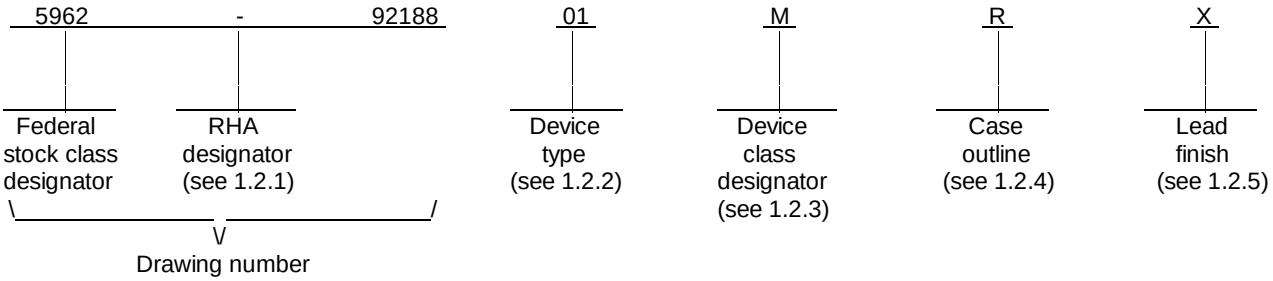
SIZE	CAGE CODE	
A	**67268**	**5962-92188**

SHEET 1 OF 25

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACTQ373	Octal transparent latch with three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Leadless-chip-carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
DC input clamp current (I_{IK}) (V_{IN} = -0.5 V and V_{CC} + 0.5 V)	±20 mA
DC output clamp current (I_{OK}) (V_{OUT} = -0.5 V and V_{CC} + 0.5 V)	±20 mA
DC output current (I_{OUT}) per output pin	±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}) per pin	±400 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	500 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 1/ 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL})	0.8 V
Minimum high level input voltage (V_{IH})	2.0 V
Case operating temperature range (T_C)	-55°C to +125°C
Input edge rate ($\Delta V/\Delta t$) maximum: (from V_{IN} = 0.8 V to 2.0 V, 2.0 V to 0.8 V)	125 mV/ns
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL})	+24 mA

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 4/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature may be exceeded for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ Values will be added when they become available from the qualified source.

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of the LATCH-UP in CMOS Integrated Circuits.

JEDEC Standard No. 20 - Standardized for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, NW, Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. This is a fully characterized military detail specification and is suitable for qualification of device classes B and S to the requirements of MIL-M-38510. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Ground bounce waveforms and test circuit. The ground bounce load circuit and waveforms shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.7 Schematic circuits. The schematic circuits shall be submitted to the preparing activity prior to the inclusion of a manufacturer's device in this drawing and shall be submitted to the qualifying activity as a prerequisite for qualification for device classes B and S. All qualified manufacturer's schematics shall be maintained and available upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range. Test conditions for these specified characteristics and limits are as specified in table I. For device classes B and S, a pin-for-pin conditions and testing sequence for table I parameters shall be maintained and available upon request from the qualifying activity, on qualified devices.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.5.2 Correctness of indexing and marking for device classes B and S. For device classes B and S, all devices shall be subjected to the final electrical tests specified in table II after PIN marking (marked in accordance with MIL-M-38510) to verify that they are correctly indexed and identified by PIN. Optionally, an approved electrical test may be devised especially for this requirement.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions unless otherwise specified 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$	Device type 3/ and device class	V_{CC}	Group A subgroups	Limits 2/		Unit
						Min	Max	
High level output voltage 3006	V_{OH1}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$	All	4.5 V	1, 2, 3	4.40		V
	V_{OH2}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$	All	5.5 V	1, 2, 3	5.40		
	V_{OH3}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -24\ mA$	All	4.5 V	1	3.86		
					2, 3	3.70		
	V_{OH4}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -24\ mA$	All	5.5 V	1	4.86		
					2, 3	4.70		
	V_{OH5} 4/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ mA$	All	5.5 V	1, 2, 3	3.85		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions unless otherwise specified 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$	Device type 3/ and device class	V_{CC}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Low level output voltage 3007	V_{OL1}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ \mu A$	All	4.5 V	1, 2, 3		0.10	V
	V_{OL2}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ \mu A$	All	5.5 V	1, 2, 3		0.10	
	V_{OL3}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 24\ mA$	All	4.5 V	1		0.36	
					2, 3		0.50	
	V_{OL4}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 24\ mA$	All	5.5 V	1		0.36	
					2, 3		0.50	
	V_{OL5} 4/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ mA$	All	5.5 V	1, 2, 3		1.65	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions unless otherwise specified 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$	Device type 3/ and device class	V_{CC}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Three-state output leakage current high 3021	I_{OZH} 5/	$\overline{OE} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $V_{OUT} = 5.5\ V$	All	5.5 V	1		0.5	µA
					2, 3		10.0	
Three-state output leakage current low 3020	I_{OZL} 5/	$\overline{OE} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $V_{OUT} = GND$	All	5.5 V	1		-0.5	µA
					2, 3		-10.0	
Positive input clamp voltage 3022	V_{IC+}	$V_{CC} = GND$ For input under test $I_{IN} = 1\ mA$	All B, S, Q, V		1	0.4	1.5	V
Negative input clamp voltage 3022	V_{IC-}	$V_{CC} = Open$ For input under test $I_{IN} = -1\ mA$	All B, S, Q, V		1	-0.4	-1.5	V
Input current high 3010	I_{IH}	For input under test $V_{IN} = V_{CC}$ For all other inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	1		0.1	µA
					2, 3		1.0	
Input current low 3009	I_{IL}	For input under test $V_{IN} = GND$ For all other inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	1		-0.1	µA
					2, 3		-1.0	
Input capacitance 3012	C_{IN}	See 4.4.1d $T_C = +25°C$	All	GND	4		10	pF
Power dissipation capacitance	C_{PD} 6/		All	5.0 V	4		50	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions unless otherwise specified 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$	Device type 3/ and device class	V_{CC}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} 7/	For input under test $V_{IN} = V_{CC} - 2.1\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	1		1.0	mA
					2, 3		1.6	
Quiescent supply current, output high 3005	I_{CCH}	$\overline{OE}$ = GND For all other inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	1		8.0	µA
					2, 3		160	
Quiescent supply current, output low 3005	I_{CCL}		All	5.5 V	1		8.0	µA
					2, 3		160	
Quiescent supply current, output three-state 3005	ICCZ 5/	$\overline{OE} = V_{CC}$ For all other inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	1		8.0	µA
					2, 3		160	
Low level ground bounce noise	V_{OLP} 8/	$V_{IH} = 3.0\ V$ $V_{IL} = 0.0\ V$ $T_A = +25°C$ See figure 4	All	5.0 V	4		1500	mV
Low level ground bounce noise	V_{OLV} 8/		All	5.0 V	4		-1200	mV
High level V_{CC} bounce noise	V_{OHP} 8/		All	5.0 V	4		V_{OH} +1000	mV
High level V_{CC} bounce noise	V_{OHV} 8/		All	5.0 V	4		V_{OH} -1800	mV
Latch-up input/ output over-voltage	I_{CC} (O/V1) 9/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $V_{over} = 10.5\ V$	All B, S, Q, V	5.5 V	2		200	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions unless otherwise specified 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$	Device type 3/ and device class	V_{CC}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Latch-up input/ output positive over-current	I_{CC} (O/I1+) 9/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $I_{trigger} = +120\ mA$	All B, S, Q, V	5.5 V	2		200	mA
Latch-up input/ output negative over-current	I_{CC} (O/I1-) 9/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $I_{trigger} = -120\ mA$	All B, S, Q, V	5.5 V	2		200	mA
Latch-up supply over-voltage	I_{CC} (O/V2) 9/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $V_{over} = 9.0\ V$	All B, S, Q, V	5.5 V	2		100	mA
Truth table test output voltage 3014	10/	$V_{IL} = 0.8\ V$ $V_{IH} = 2.0\ V$ Verify output V_O	All	4.5 V	7, 8	L	H	
			All	5.5 V	7, 8	L	H	
Propagation delay time, data to output, Dn to On 3003	t_{PHL}, t_{PLH} 11/	$C_L = 50\ pF$ minimum $R_L = 500\Omega$ See figure 5	All B, S, Q, V	4.5 V	9, 11	1.0	9.5	ns
					10	1.0	10.5	
			All M		9	1.0	9.5	
					10, 11	1.0	10.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions unless otherwise specified 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$	Device type 3/ and device class	V_{CC}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Propagation delay time, enable to output, LE to On 3003	t_{PLH}, t_{PHL} 11/	$C_L = 50$ pF minimum $R_L = 500\Omega$ See figure 5	All B, S, Q, V	4.5 V	9, 11	1.0	10.5	ns
					10	1.0	11.5	
			All M		9	1.0	10.5	
					10, 11	1.0	11.5	
Propagation delay time, output enable, OE to On 3003	t_{PZH}, t_{PZL} 11/		All B, S, Q, V	4.5 V	9, 11	1.0	9.5	ns
					10	1.0	11.0	
			All M		9	1.0	9.5	
					10, 11	1.0	11.0	
Propagation delay time, output disable, OE to On 3003	t_{PHZ}, t_{PLZ} 11/	$C_L = 50$ pF minimum $R_L = 500\Omega$ See figure 5	All B, S, Q, V	4.5 V	9, 11	1.0	9.5	ns
					10	1.0	10.5	
			All M		9	1.0	9.5	
					10, 11	1.0	10.5	
Minimum setup time Dn to LE	t_s 12/	$C_L = 50$ pF minimum $R_L = 500\Omega$ See figure 5	All B, S, Q, V	4.5 V	9, 10, 11	3.5		ns
			All M		9, 10, 11	3.5		
Minimum hold time Dn from LE	t_h 12/	$C_L = 50$ pF minimum $R_L = 500\Omega$ See figure 5	All B, S, Q, V	4.5 V	9, 10, 11	1.5		ns
			All M		9, 10, 11	1.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions unless otherwise specified 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$	Device type 3/ and device class	V_{CC}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Minimum latch enable high pulse width	t_w 12/	C_L = 50 pF minimum R_L = 500Ω See figure 5	All B, S, Q, V	4.5 V	9, 10, 11	5.0		ns
			All M		9, 10, 11	5.0		

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ Each input/output, as applicable shall be tested at the specified temperature for the specified limits. The V_{IH} minimum and V_{IL} maximum thresholds for any input that may affect the logic state of the output under test shall be verified during each V_{OL} and V_{OH} test. On some devices, this will require repeating the same V_{OL} and V_{OH} tests multiple times to verify all input thresholds. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. V_{IC} (pos) tests, the GND terminal can be open. $T_C = +25°C$.

b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. $T_C = +25°C$.

c. All I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

Additional detailed information on qualified devices (i.e., pin for pin conditions and testing sequence) is available from the qualifying activity (DESC-EQM) upon request. For negative and positive voltage and current values: The sign designates the potential difference in reference to GND and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. Devices shall meet or exceed the limits specified in table I if tested at $4.5\ V \le V_{CC} \le 5.5\ V$.

3/ Unless otherwise specified, the word "All" in the device type and device class column means the test is for all device types and classes.

4/ Transmission driving tests are performed at V_{CC} = 5.5 V dc with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for V_{IN} = 2.0 V or 0.8 V.

5/ Three-state output conditions are required.

6/ Power dissipation capacitance (C_{PD}) determines the power consumption, $P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$. The current consumption, $I_S = (C_{PD} + C_L) V_{CC} f + I_{CC} + n \times d \times \Delta I_{CC}$. For both P_D and I_S: n is the number of device inputs at TTL levels, f is the frequency of the input signal; and d is the duty cycle of the input signal.

7/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ -2.1 V (alternate method). Classes B, S, Q, and V shall use the preferred method. When the test is performed using the alternate test method: the maximum limits is equal to the number of inputs at a high TTL input level times 1.0 mA or 1.6 mA, as applicable; and the preferred method and limits are guaranteed.

8/ This test is for qualification only. Ground and V_{CC} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500 Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 4). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than .25 inches. Decoupling capacitors shall be placed in parallel from V_{CC} to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and V_{CC} bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal V_{OH} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OH} as all other outputs possible are switched from V_{OH} to V_{OL}. V_{OHV} and V_{OHP} are then measured from the nominal V_{OH} level to the largest negative and positive peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from V_{OL} to V_{OH}.

The device inputs shall be conditioned such that all outputs are at a low nominal V_{OL} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OL} as all other outputs possible are switched from V_{OL} to V_{OH}. V_{OLP} and V_{OLV} are then measured from the nominal V_{OL} level to the largest positive and negative peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from V_{OH} to V_{OL}.

9/ See JEDEC STD. 17 for electrically induced latch-up test methods and procedures. The values listed for $V_{trigger}$, $I_{trigger}$ and V_{over}, are to be accurate within ±5 percent.

10/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. H ≥ 2.5 V, L < 2.5 V.

11/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum propagation delay time limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guard-banding the V_{CC} = 4.5 V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

12/ For device class M, this parameter shall be guaranteed, if not tested, to the limits in table I, herein.

Device type	01	
Case outlines	R, S	2
Terminal number	Terminal symbol	
1	$\overline{OE}$	$\overline{OE}$
2	O0	O0
3	D0	D0
4	D1	D1
5	O1	O1
6	O2	O2
7	D2	D2
8	D3	D3
9	O3	O3
10	GND	GND
11	LE	LE
12	O4	O4
13	D4	D4
14	D5	D5
15	O5	O5
16	O6	O6
17	D6	D6
18	D7	D7
19	O7	O7
20	V_{CC}	V_{CC}

Pin descriptions	
Terminal symbol	Description
Dn (n = 0 to 7)	Data inputs
On (n = 0 to 7)	Outputs (non-inverting)
$\overline{OE}$	Output enable control input
LE	Latch enable control input

FIGURE 1. Terminal connections.

Device type 01				
Inputs			Internal	Output
LE	$\overline{OE}$	Dn	$\overline{O}$	On
H	H	L	H	Z
H	H	H	L	Z
↓	H	l	H	Z
↓	H	h	L	Z
L	H	X	NC	Z
H	L	L	H	L
H	L	H	L	H
↓	L	l	H	L
↓	L	h	L	H
L	L	X	NC	NC

H = High voltage level
L = Low voltage level
Z = High impedance
↓ = High-to-low transition
l = Low voltage level meeting the setup and hold times in table I relative to the transition of LE
h = High voltage level meeting the setup and hold times in table I relative to the transition of LE
X = Immaterial
NC = No change

FIGURE 2. Truth table.

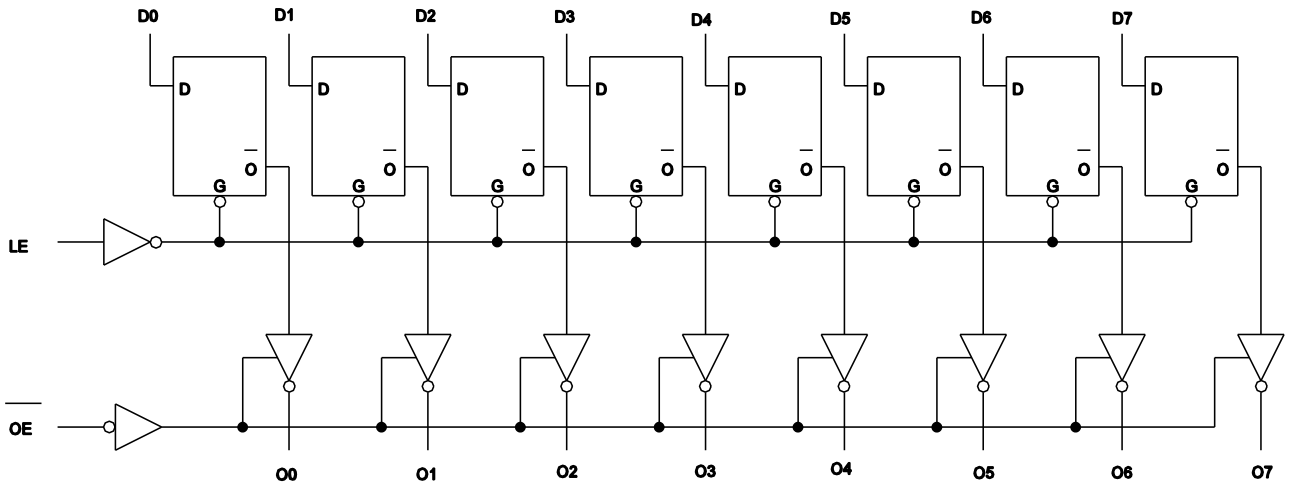
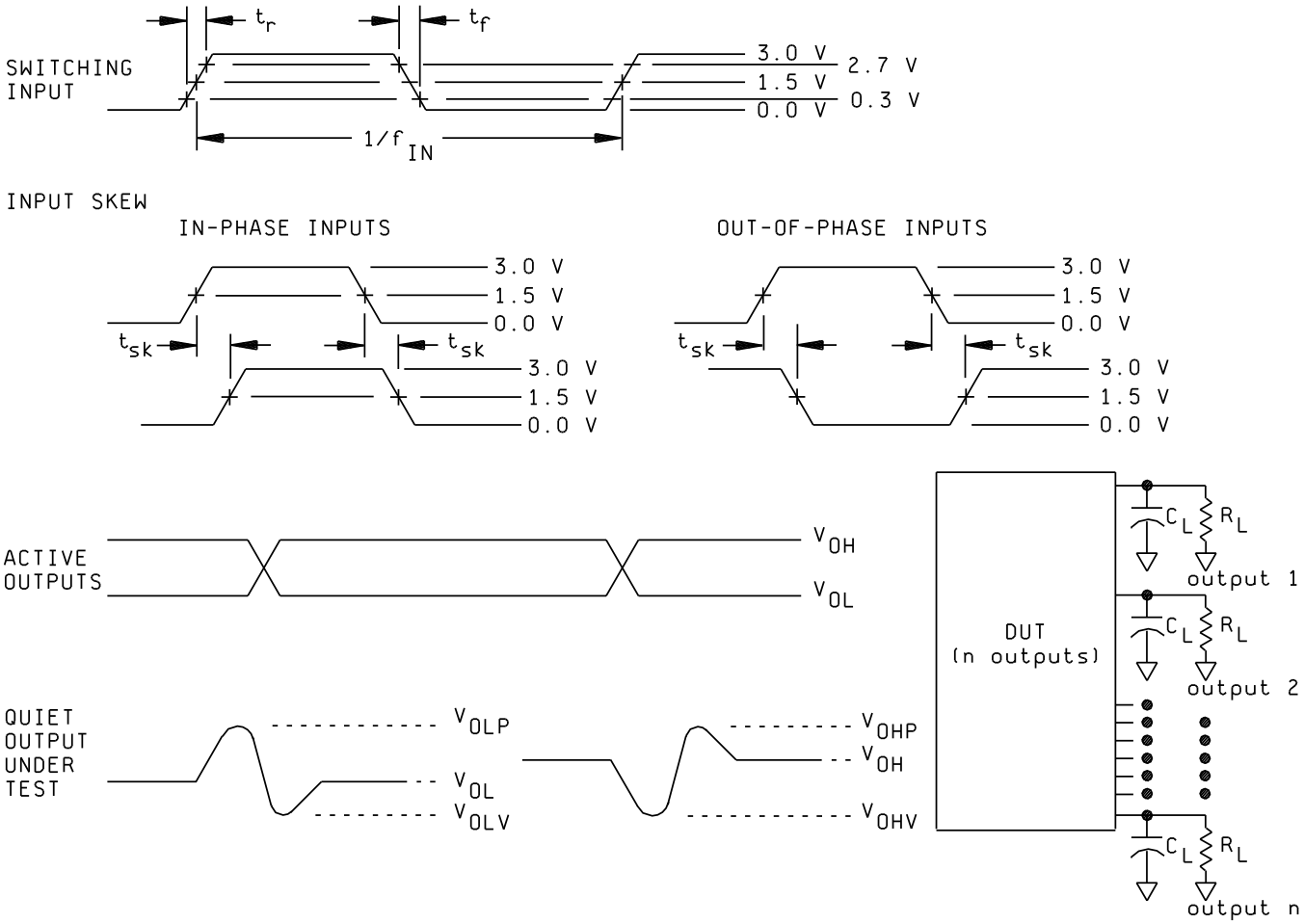


FIGURE 3. Logic diagram.



NOTES:

1. C_L includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. R_L = 450Ω ±1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
   a. V_{IN} = 0.0 V to 3.0 V; duty cycle = 50 percent; $f_{IN} \geq$ 1 MHz.
   b. t_r, t_f = 3 ns ±1.0 ns. For input signal generators incapable of maintaining these values of t_r and t_f, the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 3.0 ns ±1.0 ns; skew between any two switching inputs signals (t_{sk}): ≤ 250 ps.

FIGURE 4. Ground bounce waveforms and test circuit.

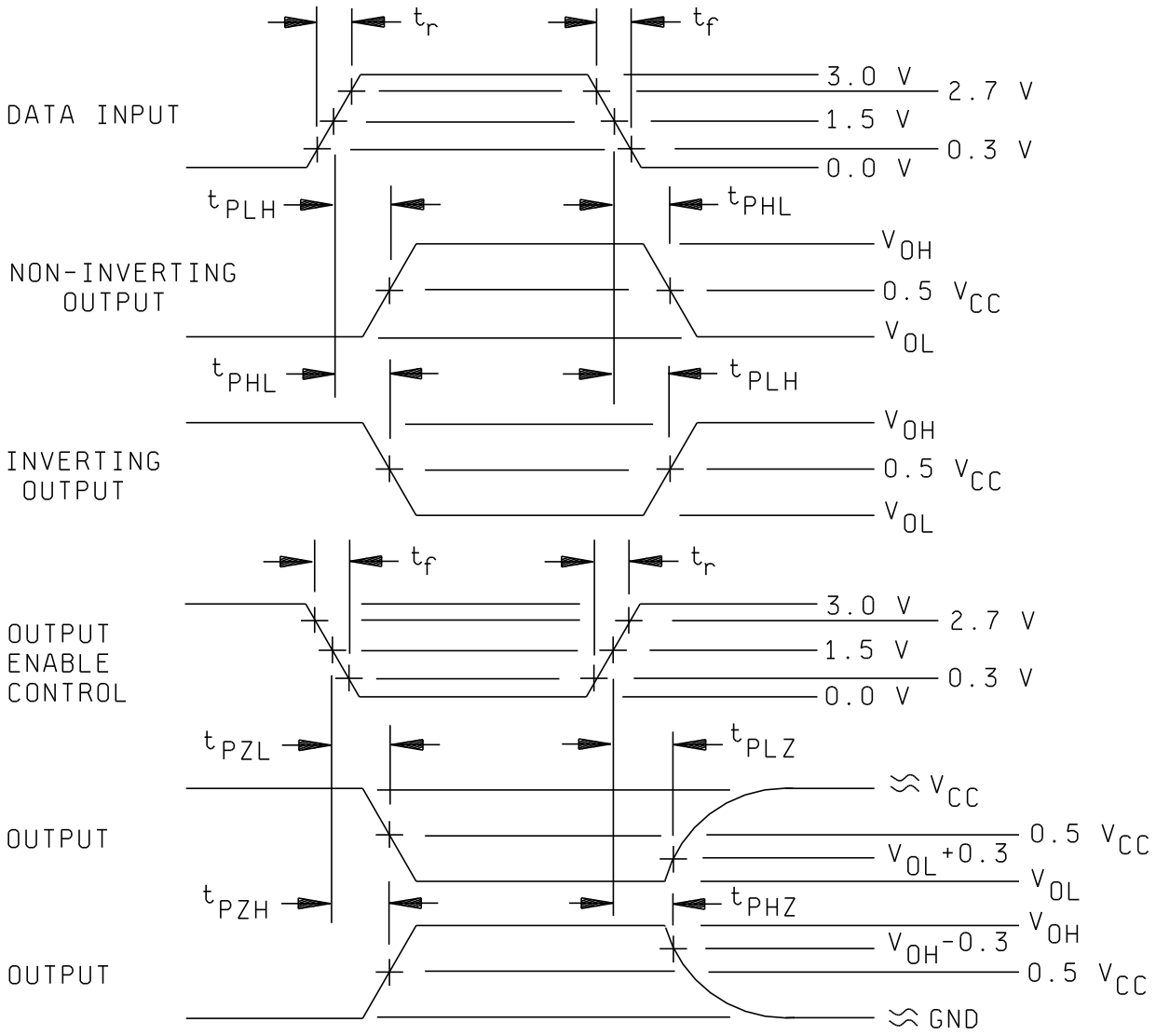
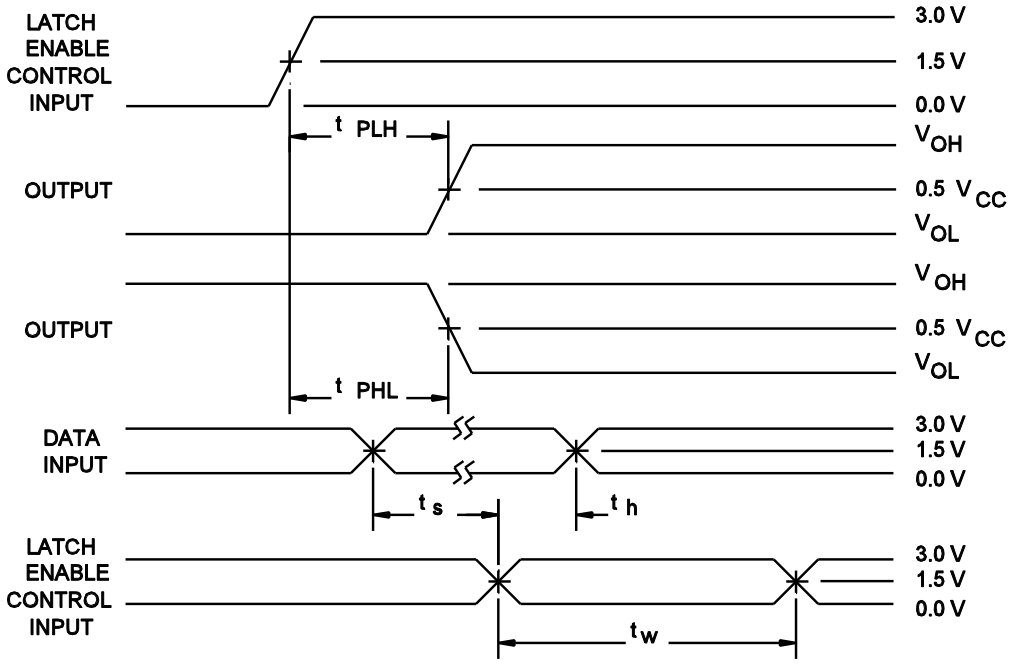
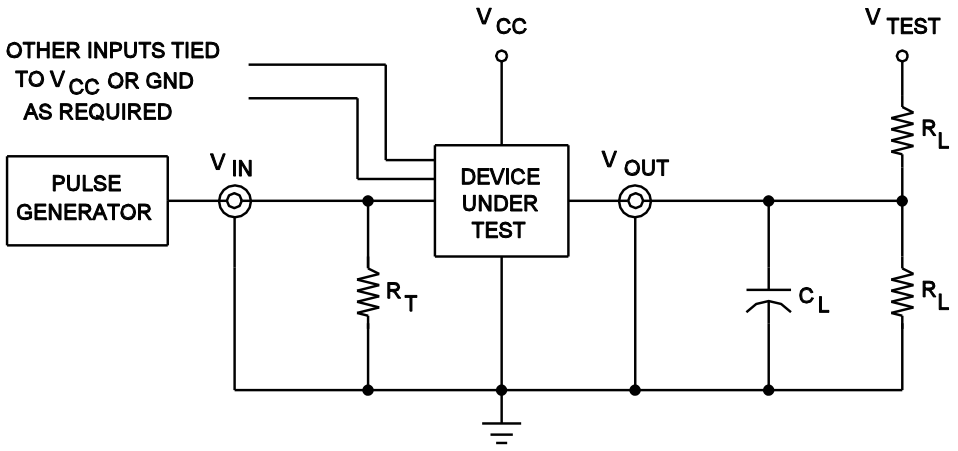


FIGURE 5. Switching waveforms and test circuit.





NOTES:
1. When measuring t_{PLZ} and t_{PZL}: $V_{TEST} = 2 \times V_{CC}$.
2. When measuring t_{PHZ}, t_{PZH}, t_{PLH} and t_{PHL}: V_{TEST} = open.
3. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
4. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
5. R_L = 500Ω or equivalent.
6. R_T = 50Ω or equivalent.
7. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; $t_r \leq 3$ ns; $t_f \leq 3$ ns; t_r and t_f shall be measured from 0.3 to 2.7 V and 2.7 V to 0.3 V, respectively; duty cycle = 50%.
8. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
9. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit - Continued.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 38 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device class B, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device class S, sampling and inspection procedures shall be in accordance with MIL-M-38510, and methods 5005 and 5007 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.1.1 Burn-in and life test circuits. For device classes B and S, the burn-in and life test circuits shall be constructed so that the devices are stressed at the maximum operating conditions stated in 4.2.1a5 or 4.2.1a6 as applicable, or equivalent as approved by the qualifying activity.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. The following additional criteria shall apply.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

(3) Delete the sequence specified in 3.1.10 through 3.1.14 of method 5004 and substitute the first 7 test requirements of table II herein.

(4) For device class M, unless otherwise noted, the requirements for device class B in method 1015 of MIL-STD-883 shall be followed.

(5) Static burn-in, device classes B and S, test condition A, test method 1015 of MIL-STD-883. The test duration for each static test shall be 24 hours minimum for class S devices and in accordance with table I of method 1015 for class B devices.

(a) For static burn-in I, all inputs shall be connected to GND. Outputs may be open or connected to $V_{CC}/2$ ±0.5 V. Resistors R1 are optional on both inputs and open outputs, and required on outputs connected to $V_{CC}/2$ ±0.5 V. R1 = 220Ω to 47 kΩ.

(b) For static burn-in II, all inputs shall be connected through the R1 resistors to V_{CC}. Outputs may be open or connected to $V_{CC}/2 \pm 0.5$ V. Resistors R1 are optional on open outputs, and required on outputs connected to $V_{CC}/2 \pm 0.5$ V. R1 = 220Ω to 47 kΩ.

(c) V_{CC} = 5.5 V +0.5 V, -0.00 V.

(6) Dynamic burn-in, device classes B and S, test condition D, method 1015 of MIL-STD-883,

(a) Input resistors = 220 Ω to 2 kΩ ±20 percent.

(b) Output resistors = 220 Ω ±20 percent.

(c) V_{CC} = 5.5 V +0.5 V, -0.00 V.

(d) The output enable control pin shall be connected through a resistor to GND. The Latch enable control pin shall be connected through a resistor to V_{CC}. All other inputs shall be connected through the resistors in parallel to a common clock pulse (CP). Outputs shall be connected to $V_{CC}/2 \pm 0.5$ V through the resistors.

(e) CP = 25 kHz to 1 MHz square wave; duty cycle = 50 percent ±15 percent; V_{IH} = 4.5 V to V_{CC}, V_{IL} = 0 V ±0.5 V; t_r, $t_f \leq 100$ ns.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. For class S devices, post dynamic burn-in, or class B devices, post static burn-in, electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. Static burn-in I and II failures shall be cumulative for determining the PDA.

c. The PDA for class B devices shall be in accordance with MIL-M-38510 for static burn-in. Dynamic burn-in is not required.

d. The PDA for class M devices shall be in accordance with MIL-M-38510 for static burn-in and dynamic burn-in.

e. Those devices whose measured characteristics, after burn-in, exceed the specified delta limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified number of failed devices times 100 divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

TABLE II. Electrical test requirements.

Test requirements, MIL-STD-883 test method (one part - one part number reference paragraph)	Subgroups 1/ (per method 5005, table I)			Subgroups 1/ (per MIL-I-38535, table III)	
	Device class M	Device class B 2/	Device class S 2/	Device class Q	Device class V
Interim electrical parameters, method 5004		1	1	1	1
Static burn-in I, method 1015 (4.2.1a)	3/	Not required	Required 4/	Not required	Required 4/
Interim electrical parameters, method 5004 (4.2.1b)			1 5/		1 5/
Static burn-in II, method 1015 (4.2.1a)	3/	Required 6/	Required 4/	Required 6/	Required 4/
Interim electrical parameters, method 5004 (4.2.1b)		1 2/ 5/	1 2/ 5/	1 2/ 5/	1 2/ 5/
Dynamic burn-in I, method 1015 (4.2.1a)	3/	Not required	Required 4/	Not required	Required 4/
Interim electrical parameters, method 5004 (4.2.1b)			1 5/		1 5/
Final electrical parameters, method 5004	1,2,3, 7,8,9 2/	1,2,7,9 2/ 6/	1,2,7,9 2/	1,2,3,7,8,9,10 ,11 2/ 6/	1,2,3,7,8,9, 10,11 2/
Group A test requirements, method 5005 (4.4.1)	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11
Group B end-point electrical parameters, method 5005 (4.4.2)			1,2,3,7,8, 9,10,11 5/		
Group C end-point electrical parameters, method 5005 (4.4.3)	1,2,3	1,2 5/		1,2,3 5/	1,2,3,7,8, 9,10,11 5/
Group D end-point electrical parameters, method 5005 (4.4.4)	1,2,3	1,2	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters, method 5005 (4.4.5)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.

2/ PDA applies to subgroup 1 (see 4.2.3). For device classes S and V, PDA applies to subgroups 1 and 7 (see 4.2.3).

3/ The required test condition used for burn-in shall be that submitted to DESC-EC with the certificate of compliance, see 4.2.1a herein.

4/ On all class S lots, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with test method 5004 of MIL-STD-883. For preburn-in and interim electrical parameters the read-and-record requirements are for delta measurements only.

5/ Delta limits shall be required only on table I, subgroup 1. The delta values shall be computed with reference to the previous interim electrical parameters. The delta limits are specified in table III.

6/ The device manufacturer may at his option either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias; or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias). When the manufacturer elects to perform the subgroup 1 electrical parameter measurements without delta measurements, there is no requirement to perform the pre-burn-in electrical tests (first interim electrical parameters test in table II).

TABLE III. Delta limits at +25°C.

Parameter 1/	Device types	Limits
I_{CCL}, I_{CCH}, I_{CCZ}	All	±100 nA

1/ The parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.3 Electrostatic discharge sensitivity qualification inspection . Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Latch-up tests are required for all device classes. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. Test all applicable pins on five devices with zero failures.

c. Ground and V_{CC} bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to limits established for the worst case package. The package type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DESC data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

   Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DESC-EC of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DESC-EC data from testing on both fixtures, that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

d. C_{IN}, C_{OUT}, and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For C_{IN}, C_{OUT}, and C_{PD}, test all applicable pins on five devices with zero failures.

e. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

f. For device classes B and S, t_s, t_h, and t_w shall be guaranteed, if not tested, to the limits specified in Table I.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein and as follows.

a. Class S steady-state life (accelerated) shall be conducted using test condition D of method 1005 of MIL-STD-883 and the circuit described in 4.2.1a6 herein, or equivalent as approved by the qualifying activity. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

b. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table III herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table III herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition A, B, C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-M-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as specified in table I at T_A = +25°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331, and as follows:

GND	Ground zero voltage potential.
I_{CC}	Quiescent supply current.
I_{IL}	Input current low.
I_{IH}	Input current high.
T_C	Case temperature.
T_A	Ambient temperature.
V_{CC}	Positive supply voltage.
C_{IN}	Input terminal-to-GND capacitance.
C_{PD}	Power dissipation capacitance.
V_{IC+}	Positive input clamp voltage.
V_{IC-}	Negative input clamp voltage.
t_w	Trigger duration (width).
O/V	Latch-up over-voltage.
O/I	Latch-up over-current.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 93-06-07

Approved sources of supply for SMD 5962-92188 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9218801MRX	27014	54ACTQ373DMQB
5962-9218801MSX	27014	54ACTQ373FMQB
5962-9218801M2X	27014	54ACTQ373LMQB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090 Point-of-contact: 333 Western Avenue South Portland, ME 04106